ECE411 MP4 CP1

Progress Report

RV32I ISA and basic pipelining

Tingkai Liu, Zhi Cen

2020/11/11

1 Functionality and Work Distribution

|  |  |  |
| --- | --- | --- |
| Functionality | Notes | Work Distribution |
| a 5-stage pipeline cpu which can handle RV32I Instructions | 1. no hazard detection  2. full RV32I Instructions except FENCE\*, ECALL, EBREAK, and CSRR | Zhi: split mp2 cpu into 5 stages, unit test each stage and test the whole cpu with provided tb.  Tingkai: design control rom, assign control signals to each stage and connect all stages in datapath. |
|  |  |  |

2 Update Datapath

see cp1\_datapath.png

3 Update Interface

3.1 Control ROM

module control\_rom(

input rv32i\_opcode opcode,

input logic [2:0] funct3,

input logic [6:0] funct7,

output rv32i\_ctrl\_packet\_t ctrl

);

3.2 Update the design of cpu\_control

Before: get decode information from each buffer and output all control signals from cpu\_control.

Now: decode instruction by control\_rom and save them in ctrl packet. In cpu\_control, only deal with signals that can’t be determined at ID stage.

4 Testing Strategy

We wrote unit test for each stage to fix some basic bugs.

We use the rvfi monitor and provided source code to test the whole pipeline.

5 Bug log

5.1

Bug: PC didn't change at branch

Reason: forgot to set ALU for EX when BR

5.2

Bug: Invalid data read from D memory

Reason: forgot to mask the low 2 bits for mem\_addr

Note: I-cache access is always 4 byte allign so no need for that

5.3

Bug: When EX indicates halt, the WB for previous inst may not finish

Reason: The way for detecting halt may need to change

5.4

Bug: missing information for rvfimon

Reason: For rvfi monitor, we need to save additional information in packet

Note: data\_mem\_rdata == mdrreg\_out

5.5

Bug: rd\_addr doesn’t match

Reason: all signals for rvfi monitors should be sent from wb stage

Note: Only commit at wb.load\_buffers && wb.inst != nop

5.6

Bug: pc\_wdata doesn’t match at beq inst

Reason: pc\_wdata should be pc+4 or alu\_out

ECE411 MP4 CP2

Roadmap

L1 caches, hazards and static branch prediction

Tingkai Liu, Zhi Cen

2020/11/11

|  |  |  |
| --- | --- | --- |
| Functionality | Notes | Work assigned to |
| L1 cache, arbiter | 1. arbiter connected to I-Cache, D-cache and memory  2. no cache coherence | Tingkai |
| Hazard, static branch prediction | 1. data hazard: forwarding  2. control hazard: static-not-taken branch prediction | Zhi |